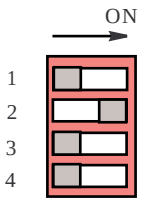
FLASH / EPROM Memory Map on DEBUG Board connected to MAIN CPU Vr4122 Harrier Board

BE00 0000 - BFBF FFFF

28 Megs Linear



S2 bit 1 off, bit 2 on

A18 address bit is toggled to Flash

Eprom is overlayed on top of flash memory

256K EPROM

256K B FLASH

256K A FLASH

BFC8 0000 - BFFF FFFF

3.5 Megs Linear

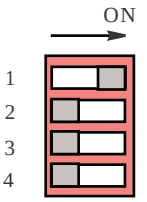
32 Megs of Flash

S2 Bit 1: EPROM / Flash select
ON - Reset vector from Flash
OFF - Reset vector is from EPROM with size of 256K bytes

S2 bit 2: A18 inverted to Flash Memory
ON: Flash memmory address 0xBFC00000-BFC3FFFF i s remapped to 0xBFC40000-BFC7FFFF, and vice versa
OFF : A18 is normal to Flash Memory

BE00 0000 - BFBF FFFF

28 Megs Linear



S2 bit 1 on, bit 2 off

A18 address bit is normal

256K A FLASH

256K B FLASH

BFC8 0000 - BFFF FFFF

3.5 Megs Linear

32 Megs of Flash

BFC0 0000

BFC3 FFFF

BFC4 0000

BFC7 FFFF

BFC8 0000

BFFF FFFF

Use these settings for testing flash with or without the Debug Board being connected

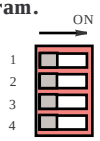
Harrier FLASH MAP Diagram

Optional setting to use 256K B Flash Boot Area with Debug board. Does not operate with just Flash on Main CPU board alone, unless the A region is also programmed with some type off BOOT program.

S2 bit 1 off, bit 2 off

A18 address bit is normal

Eprom is overlayed on top of flash memory



256K EPROM

256K A FLASH

256K B FLASH

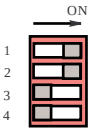
BFC0 0000

BFC3 FFFF

BFC4 0000

BFC7 FFFF

S2 bit 1 on, bit 2 on



28 Megs

256K B FLASH

256K A FLASH

3.5 Megs

MAIN board by itself Straight Linear 32 Megs of FLASH MEMORY

BE00 0000

32 Megs of Flash

BFFF FFFF

July 20, 2000 3:37pm
Harrier Flash Map.pdx